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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JOSEPH, DENNIS P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,141	SEMPEL ET AL.	
	Examiner	Art Unit	
	Dennis P. Joseph	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/525,141.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to amendments filed in application No. 10/525,141 on February 16, 2005. Claims 1,2,4-16 are pending and have been examined.

Claim Rejections – 35 USC § 103

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1,2,5-9,11-16** rejected under 35 U.S.C. 103(a) as being unpatentable over **Nishigaki et al. (US 6,310,589 B1)** in view of **Wei et al. (US 5,723,950)**

Nishigaki teaches in Claim 1:

A display device comprising at least one picture element and a display driver device (Column 1, Lines 9-12) comprising a driving transistor (Column 7, Lines 9-11, "A reference current Iref is supplied to transistors **90** and **91**." Figure 4 shows the circuit with the transistor **91**.) to be connected in series with the picture element in a first current

path (Column 4, Lines 18-19, "organic thin film EL element **20**" Figure 4 shows the element **20** to be in series with the transistor **91**.), but

Nishigaki does not explicitly teach that "the display driver comprising means for monitoring and controlling the current in said first current path, wherein the means for monitoring include an amplifier having a first input connected to the first current path, a second input connected to a second current path, and an output connected to a controlling connection of the driving transistor"

However, in the same field of endeavor, displays for luminescent devices, Wei teaches of a pre-charge circuit 40' which includes an operational amplifier 46'. As seen from Figure 3, it has a first current path connected to the negative input, a second current path connected to the positive input, and the output which is output to the driving transistor 25' (Wei, Column 4 Lines 17-38)

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the pre-charge circuit as taught by Wei with Nisigaki's driver circuit by implementing the circuit with the motivation that less current, power is required and less capacitance is incurred by having a pre-charge circuit. (Wei, Column 1, Lines 60-67)

Wei teaches in Claim 2:

The display device as claimed in claim 1 wherein operation the current in the first current path is controlled by a current simultaneously passing in the second current path. (Figure 3 shows the second current path, connected to the positive terminal and is controlling the current in the first current path, connected to the negative terminal)

Wei teaches in Claim 5:

A display device (Column 1, Lines 10-13) as claimed in claim 1, wherein, in operation, the current in the first current path is controlled by a charge stored by means of a current having passed in the second current path. (Figure 3 shows the capacitor 45' used for storing charge and this is in the second current path)

Wei teaches in Claim 6:

The display device as claimed in claim 1, wherein one of the first input and the second input of the control amplifier is coupled to a capacitor storing a control charge (Figure 3 shows the capacitor 45' used for storing charge and this is in the second current path)

Wei teaches in Claim 7:

The display device as claimed in claim 1, wherein the first input of the control amplifier is coupled to the first current path and the second input of the control amplifier is coupled to a capacitor storing a control charge. (Figure 3 shows the first input connected to the negative input of 46 and the second input connected to the positive input which contains the capacitor 45')

Wei teaches in Claim 8:

The display device as claimed in claim 1, wherein the picture element is a luminescent element and the first current determines a luminescence of the luminescent element. (Column 2, Lines 32-35)

Nishigaki teaches in Claim 9:

A display driver device (Column 1, Lines 9-12) comprising:

a driving transistor for driving (Column 7, Lines 9-11, "A reference current Iref is supplied to transistors **90** and **91**." Figure 4 shows the circuit with the transistor **91**.), a picture element (EL element), but

Nishigaki does not explicitly teach that the picture element "via a first current path the first current path being controllable by a current in a second current path related to an input data value for the picture element, and a control amplifier, a controlling connection of the driving transistor being coupled to an output of the control amplifier, a first input of the control amplifier being coupled to the first current path, a second input of the control amplifier being connected to a second current path, and an output of the control amplifier being connected to a controlling connecting of the driving transistor."

However, in the same field of endeavor, displays for luminescent devices, Wei teaches of a pre-charge circuit 40' which includes an operational amplifier 46'. As seen from Figure 3, it has a first current path connected to the negative input, a second current path

connected to the positive input, and the output which is output to the driving transistor 25' (Wei, Column 4 Lines 17-38)

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the pre-charge circuit as taught by Wei with Nisigaki's driver circuit by implementing the circuit with the motivation that less current, power is required and less capacitance is incurred by having a pre-charge circuit. (Wei, Column 1, Lines 60-67)

Nishigaki teaches in Claim 11:

The display driver device as claimed in claim 9, wherein the second current path comprises a current source. (Figure 1 shows the constant current supply **22**.)

Nishigaki teaches in Claim 12:

A display driver device comprising:

A driving transistor for driving a picture element via a first current path (Figure 4 shows driving transistor **91**) wherein, in operation, the current in the first current path is controlled by a charge stored by means of a current having passed in a second circuitry part, but

Nishigaki does not explicitly teach driving "via a first current path in which in operation the current in the first current path is controlled by a charge stored by means of a current having passed in a second circuitry part" or of a "A control amplifier having an output

coupled to the of the driving transistor, a first input of the control amplifier being coupled to the first current path, and a second input of the control amplifier being connected to a second current path."

However, in the same field of endeavor, displays for luminescent devices, Wei teaches of a pre-charge circuit 40' which includes an operational amplifier 46'. As seen from Figure 3, it has a first current path connected to the negative input, a second current path connected to the positive input, and the output which is output to the driving transistor 25' (Wei, Column 4 Lines 17-38) Furthermore, Wei discloses in Figure 3 of a capacitor 45' used for storing the charge and this is in the second current path and has an effect on the first current path.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the pre-charge circuit as taught by Wei with Nisigaki's driver circuit by implementing the circuit with the motivation that less current, power is required and less capacitance is incurred by having a pre-charge circuit. (Wei, Column 1, Lines 60-67)

Wei teaches in Claim 13:

The display driver device as claimed in claim 12, wherein a controlling connection of the driving transistor is coupled to the output of a control amplifier (Figure 3 shows the output of the amplifier to be connected to transistor 25'), and one of the first input and the second input of the control amplifier is coupled to a capacitor storing the

control charge. (Figure 3, The second current path, connected to the positive terminal is connected to a capacitor 45' for storing a charge)

Wei teaches in Claim 14:

The display driver device of claim 6, wherein the control charge is stored by means of a current having passed in the second current path. (Figure 3 shows the second current path, connected to the positive terminal and is controlling the current in the first current path, connected to the negative terminal)

Wei teaches in Claim 15:

The display driver device of claim 1, wherein the first input is an inverting input and the second input is a non-inverting input. (Figure 3 shows the first input to be inverting and the second to be non-inverting for the amplifier 46')

Wei teaches in Claim 16:

The display driver device of claim 9, wherein the first input is an inverting input and the second input is a non-inverting input. (Figure 3 shows the first input to be inverting and the second to be non-inverting for the amplifier 46')

4. **Claims 4 and 10** rejected under 35 U.S.C. 103(a) as being unpatentable over **Nishigaki et al. (US 6,310,589 B1)** and **Wei et al. (US 5,723,950)** as applied to claims 2 and 9 above, and further in view of **Inoue (US 6,469,455 B1)**

Nishigaki teaches in Claim 4:

The display device (Column 1, Lines 9-12) as claimed in claim 2, wherein the driving transistor (Column 7, Lines 9-11, transistor 91), but

Nishigaki does not explicitly teach the driving transistor "is a field effect transistor, and the controlling connecting is a gate of the field effect transistor."

However, in the same field of endeavor, displays for luminescent devices, Inoue teaches "the current switch 3 and boosting switch 5 are constituted of MOSFET's, and the operations of respective MOSFET's are controlled in accordance with the data signal DATA and reversed data signal XDATA so as to switch the electric current path of the circuit to thereby conduct the charge and discharge of the capacitor **4**." (Inoue, Column 9, Lines 55-60) Figure 1 shows the switch **3** to drive the signal to LD **2**. The output is connected to the light emitting element 2 and the gate is the controlling connection.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the MOSFET as taught by Inoue with Nishigaki's circuit, as modified by Wei, with the motivation that the MOSFET "reduces the conventional unstable operation of the current source 1 due to charging and discharging of the capacitor **4**, thereby enabling the stable high speed modulation of the light emitting element **2**." (Inoue, Column 9, Lines 65-67)

Nishigaki teaches in Claim 10:

The display driver device (Column 1, Lines 9-12) as claimed in claim 9, wherein the driving transistor (Column 7, Lines 9-11, "A reference current Iref is supplied to transistors **90** and **91**." Figure 4 shows the circuit with the transistor **91**.)

Nishigaki does not explicitly teach the driving transistor "being a field effect transistor, and the controlling connection is a gate of the field effect transistor."

However, in the same field of endeavor, displays for luminescent devices, Inoue teaches "the current switch 3 and boosting switch 5 are constituted of MOSFET's, and the operations of respective MOSFET's are controlled in accordance with the data signal DATA and reversed data signal XDATA so as to switch the electric current path of the circuit to thereby conduct the charge and discharge of the capacitor **4**." (Inoue, Column 9, Lines 55-60) Figure 1 shows the switch **3** to drive the signal to LD **2**. The output is connected to the light emitting element 2 and the gate is the controlling connection.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the MOSFET as taught by Inoue with Nisigaki circuit, as modified by Wei, with the motivation that the MOSFET "reduces the conventional unstable operation of the current source 1 due to charging and discharging of the capacitor **4**, thereby enabling the stable high speed modulation of the light emitting element **2**." (Inoue, Column 9, Lines 65-67)

Response to Arguments

5. Applicant's arguments considered, but are considered moot on ground of new rejection.

Applicant argued the amplifier had an output connected to a controlling connection of the driving transistor. The new rejection includes Wei, who teaches of an amplifier 46' whose output is connected to a driving transistor 25' for controlling the brightness of the LED.

Conclusions

6. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure. **Kawakami et al. (5,949,194), Tam (US 2002/0047817 A1), Mikami et al. (US 2002/0140659 A1), Tam (US 2003/0117082 A1), Pramanik (US 2002/0082799 A1), Weindorf (US 2002/0135572 A1)** are cited to teach of an amplifier with current inputs which control the output to an LED.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

AMR A. AWAD
SUPERVISORY PATENT EXAMINER